METHOD AND SYSTEM FOR FLEXIBLY NESTING JTAG TAP CONTROLLERS FOR FPGA-BASED SYSTEM-ON-CHIP (SoC)

ABSTRACT

A flexible architecture for nesting joint test action group (JTAG) test access port (TAP) controllers for FPGA-based embedded system-on-chip (SoC) is provided. Advantageously, a programmable approach permits bits in a selectable bit register (302) to be selected based on the number of JTAG TAPs that will be utilized. The selected bits can be used to vary the apparent length of an instruction register (302). Importantly, the flexible architecture permits access to any combination of a plurality of JTAG TAP controllers in the FPGA-based embedded SoC without the need to rewire any I/O pins of the FPGA and/or embedded IP cores.